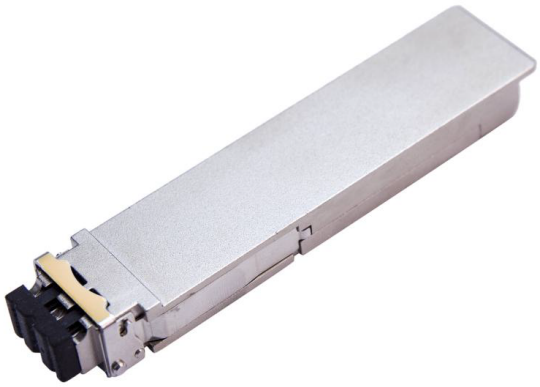
**CL-CF4-SR4**
**100G CFP4 Optical Transceiver Module**
**RoHS 6 compliant**



## Features

- Hot pluggable CFP4 MSA form factor
- Compliant to IEEE 802.3bm 100GBASE-SR4
- Supports 103.1Gb/s aggregate bit rate
- Up to 300m OM4 MMF transmission
- Single +3.3V power supply
- Operating case temperature: -5 to 70oC
- 4x25G electrical interface (OIF CEI-28G-VSR)
- MDIO management interface with digital diagnostic monitoring
- Maximum power consumption 3.5W
- MTP/MPO optical connector
- RoHS-6 compliant

## Applications

- 100GBASE-SR4 Ethernet

| PART NUMBER | Monitor | INPUT/OUTPUT | SIGNAL DETECT | TEMPERATURE |
|---|---|---|---|---|
| CL-CF4-SR4 | X | AC/AC | TTL | -5°C to 70 °C |
| CL-CF4-SR4i | X | AC/AC | TTL | -40°C to 85 °C |

**CL-CF4-SR4**
**100G CFP4 Optical Transceiver Module**
**RoHS 6 compliant**

## Description

This product is a 100Gb/s transceiver module for optical communication applications compliant to 100GBASE-SR4 of the IEEE P802.3bm standard. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of VCSEL optical signals over 4 multimode fibers for 100Gb/s optical transmission. Reversely, on the receiver side, the module receives 4 channels of VCSEL optical signals over 4 multimode fibers and then converts them to 4 output channels of 25Gb/s electrical data.
The high speed VCSEL transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 300m links over OM4 multimode fibers and compliant to optical interface with IEEE802.3bm Clause 95 100GBASE-SR4 requirements.
The product is designed with form factor, optical/electrical connection and MDIO interface according to the CFP4 Multi-Source Agreement (MSA). The innovative design has all the fibers inside the CFP4 package configured without any splicing or non-permanent connector. Also, fiber routines are neatly organized and fixed inside a stainless steel container.

### Functional Description

This product contains an MTP/MPO optical connector for the optical interface and a 56-pin connector for the electrical interface. Figure 1 in Section 3 shows the functional block diagram of this product.

### Transmitter Operation

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock and Data Recovery (CDR) which reshapes and reduces the jitter of each electrical signal. Subsequently, each channel of the 4-channel laser driver converts one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 VCSEL lasers which are packaged in the optical engine. Each laser launches an optical signal whose characteristics are compliant to IEEE802.3bm 100GBASE-SR4 requirements. The transmitter output can be turned off by TX_DIS hardware signal and/or through MDIO module management interface.

### Receiver Operation

The receiver receives 4 channels of VCSEL optical signals over 4 multimode fibers and each of the 4 channels of optical signals is fed into one of the 4 receivers that are packaged in the optical engine. Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by a 4-channel CDR. The retimed 4-lane output electrical signals are compliant with OIF CEI-28G-VSR interface requirements. In addition, each received optical signal is monitored by the DOM. The monitored value is reported through the MDIO section.
If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

### MDIO Interface

The CFP4 module supports the MDIO interface specified in IEEE802.3bm Clause 45. It supports alarm, control and monitor functions via hardware pins and via an MDIO bus. Upon module initialization, these functions are available. CFP4 MDIO electrical interface consists of 6 wires including 2 wires of MDC and MDIO, as well as 3 Port Address wires, and the Global Alarm wire. MDC is the MDIO Clock line driven by host and MDIO is the bidirectional data line driven by both host and module depending upon the data directions. The CFP4 uses pins in the electrical connector to instantiate the MDIO interface as listed in Table 1. MDIO Interface Pins.

**Table 1. MDIO Interface Pins**

| PIN | Symbol | Description | I/O | Logic | "H" | "L" |
|---|---|---|---|---|---|---|
| 13 | GLB_ALRMn | Global Alarm | O | 3.3V LVCMOS | OK | Alarm |
| 18 | MDIO | Management Data Input Output Bi-Directional Data | I/O | 1.2V LVCMOS | | |
| 17 | MDC | MDIO Clock | I | 1.2V LVCMOS | | |
| 19 | PRTADR0 | MDIO port address bit 0 | I | 1.2V LVCMOS | per MDIO document | |
| 20 | PRTADR1 | MDIO port address bit 1 | I | 1.2V LVCMOS | | |
| 21 | PRTADR2 | MDIO port address bit 2 | I | 1.2V LVCMOS | | |

## 3. Transceiver Block Diagram

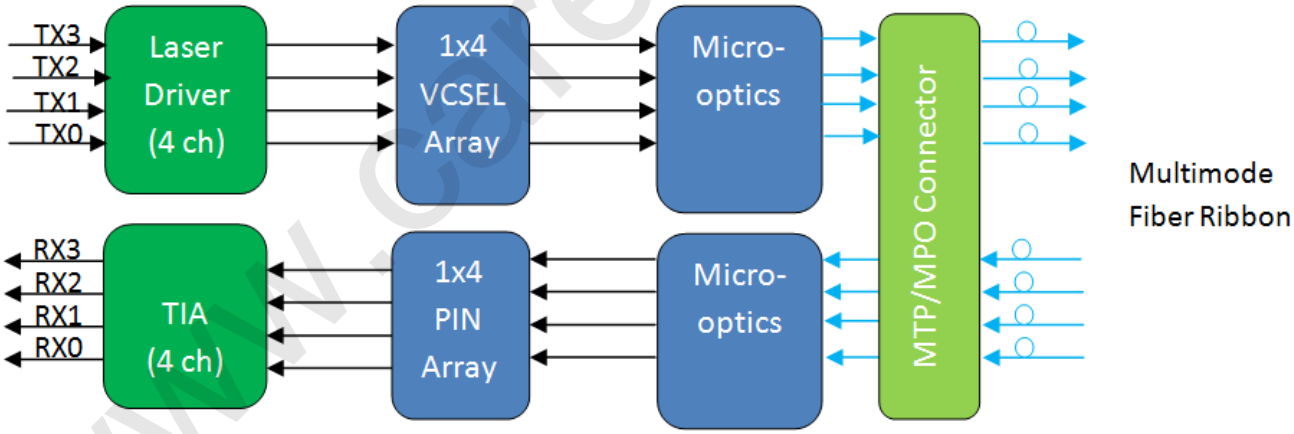



**Figure 1. 100G CFP4 SR4 Transceiver Block Diagram**

**4. Pin Assignment and Description**

The CFP4 electrical connector has 56 pins, which are arranged in top and bottom rows. The pin orientation is shown in Figure 2 and the pin map is shown in Table 2. The detailed description of the bottom side pins from pin 1 through pin 28 is shown in Table 3 while the description of the top side pins is shown in Table 4.

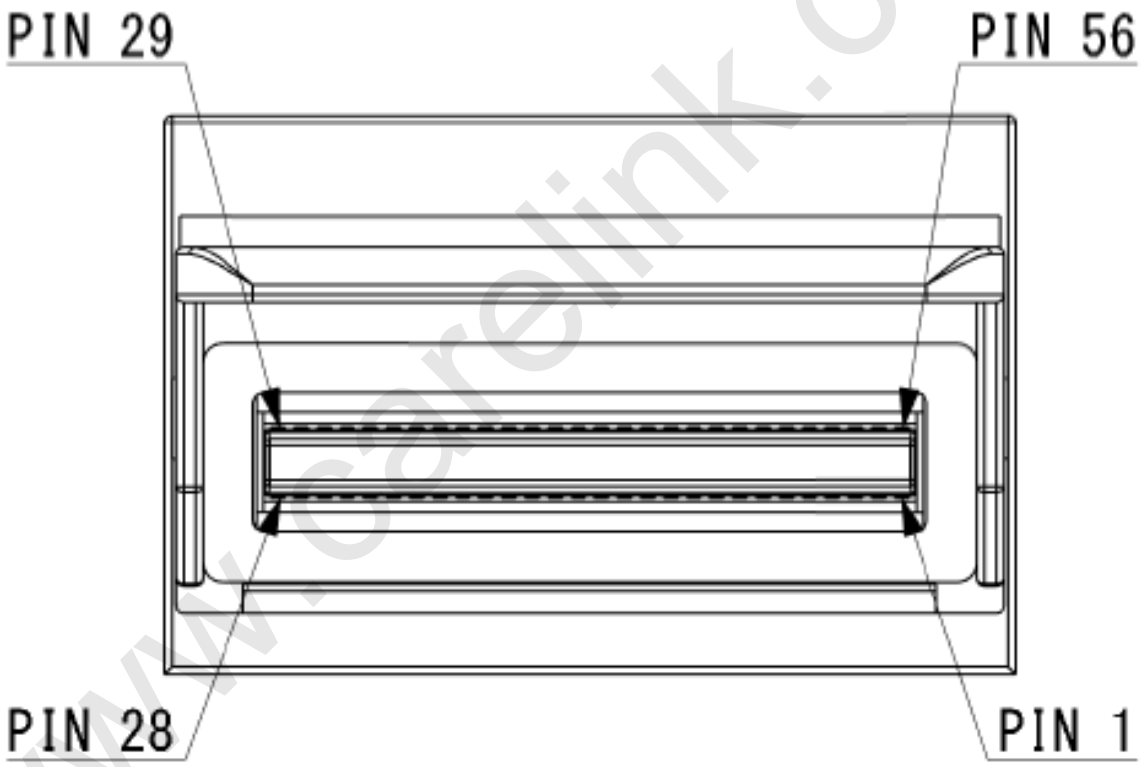



**Figure 2. CFP4 Connector Pin Map Orientation**

**Table 2. Pin Map**

| | CFP4 Bottom | | CFP4 Top |
|---|---|---|---|
| 1 | 3.3V_GND | 56 | GND |
| 2 | 3.3V_GND | 55 | TX3n |
| 3 | 3.3V | 54 | TX3p |
| 4 | 3.3V | 53 | GND |
| 5 | 3.3V | 52 | TX2n |
| 6 | 3.3V | 51 | TX2p |
| 7 | 3.3V_GND | 50 | GND |
| 8 | 3.3V_GND | 49 | TX1n |
| 9 | VND_IO_A | 48 | TX1p |
| 10 | VND_IO_B | 47 | GND |
| 11 | TX_DIS *(PRG_CNTL1)* | 46 | TX0n |
| 12 | RX_LOS *(PRG_ALRM1)* | 45 | TX0p |
| 13 | GLB_ALRMn | 44 | GND |
| 14 | MOD_LOPWR | 43 | *(REFCLKn)* |
| 15 | MOD_ABS | 42 | *(REFCLKp)* |
| 16 | MOD_RSTn | 41 | GND |
| 17 | MDC | 40 | RX3n |
| 18 | MDIO | 39 | RX3p |
| 19 | PRTADR0 | 38 | GND |
| 20 | PRTADR1 | 37 | RX2n |
| 21 | PRTADR2 | 36 | RX2p |
| 22 | VND_IO_C | 35 | GND |
| 23 | VND_IO_D | 34 | RX1n |
| 24 | VND_IO_E | 33 | RX1p |
| 25 | GND | 32 | GND |
| 26 | *(MCLKn)* | 31 | RX0n |
| 27 | *(MCLKp)* | 30 | RX0p |
| 28 | GND | 29 | GND |

**Table 3. Definition of the Bottom Side Pins from Pin 1 through Pin 28**

| PIN | Name | I/O | Logic | Description |
|---|---|---|---|---|
| 1 | 3.3V_GND | | | 3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground |
| 2 | 3.3V_GND | | | |
| 3 | 3.3V | | | |
| 4 | 3.3V | | | |
| 5 | 3.3V | | | |
| 6 | 3.3V | | | 3.3V Module Supply Voltage |
| 7 | 3.3V_GND | | | |
| 8 | 3.3V_GND | | | |
| 9 | VIND_IO_A | I/O | | Module Vendor I/O A. Do Not Connect |
| 10 | VIND_IO_B | I/O | | Module Vendor I/O B. Do Not Connect |
| 11 | TX_DIS (PRG_CNTL1) | I | LVCMOS w/PUR | Transmitter Disable for all lanes. "1" or NC: Transmitter disabled; "0": transmitter enabled. (Optionally configurable as Programmable Control1 after Reset) |
| 12 | RX_LOS (PRG_ALR M1) | O | LVCMOS w/PUR | Receiver Loss of Optical Signal. "1": low optical signal; "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset) |
| 13 | GLB_ALR Mn | O | LVCMOS | Global Alarm. "0": alarm condition in any MDIO Alarm register; "1": no alarm condition, Open Drain, Pull up Resistor on Host |
| 14 | MOD_LOP WR | I | LVCMOS w/PUR | Module Low Power Mode. "1" or NC: module in low power (safe) mode; "0": power-on enabled |
| 15 | MOD_ABS | O | GND | Module Absent. "1" or NC: module absent; "0": module present, Pull up resistor on Host |
| 16 | MOD_RSTn | I | LVCMOS w/PDR | Module Reset. "0": resets the module; "1" or NC: module enabled, Pull down Resistor in Module |
| 17 | MDC | I | 1.2V CMOS | Management Data Clock (electrical specs as per IEEE Std 802.3-2012) |
| 18 | MDIO | I/O | 1.2V CMOS | Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010) |
| 19 | PRTADR0 | I | 1.2V CMOS | MDIO Physical Port address bit 0 |
| 20 | PRTADR1 | I | 1.2V CMOS | MDIO Physical Port address bit 1 |
| 21 | PRTADR2 | I | 1.2V CMOS | MDIO Physical Port address bit 2 |
| 22 | VND_IO_C | I/O | | Module Vendor I/O C. Do Not Connect |
| 23 | VND_IO_D | I/O | | Module Vendor I/O D. Do Not Connect |
| 24 | VND_IO_E | I/O | | Module Vendor I/O E. Do Not Connect |

| | | | | |
|---|---|---|---|---|
| 25 | GND | | | |
| 26 | (MCLKn) | O | CML | For optical waveform testing. Not for normal use |
| 27 | (MCLKp) | O | CML | For optical waveform testing. Not for normal use |
| 28 | GND | | | |

**Table 4. Definition of Top Side Pins**

| PIN | Name | | PIN | Name |
|---|---|---|---|---|
| 29 | GND | | 43 | (REFCLKp) |
| 30 | RX0p | | 44 | GND |
| 31 | RX0n | | 45 | TX0p |
| 32 | GND | | 46 | TX0n |
| 33 | RX1p | | 47 | GND |
| 34 | RX1n | | 48 | TX1p |
| 35 | GND | | 49 | TX1n |
| 36 | RX2p | | 50 | GND |
| 37 | RX2n | | 51 | TX2p |
| 38 | GND | | 52 | TX2n |
| 39 | RX3p | | 53 | GND |
| 40 | RX3n | | 54 | TX3p |
| 41 | GND | | 55 | TX3n |
| 42 | (REFCLKn) | | 56 | GND |

## 5. Optical Interface Lanes and Assignment

Figure 3 shows the orientation of the multi-mode fiber facets of the optical connector. Table 5 provides the lane assignment.

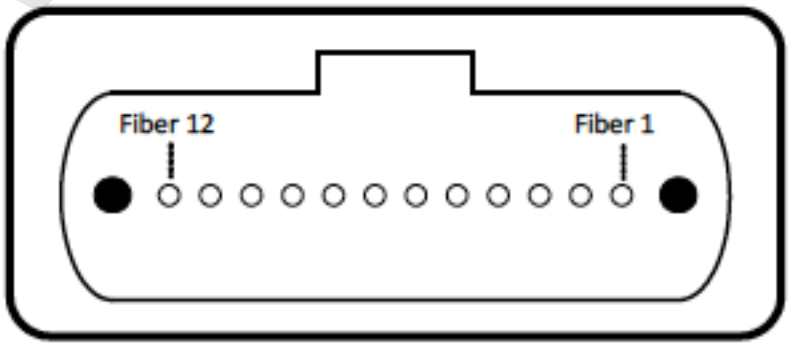



**Figure 3. Outside View of the CFP4 Module MPO Receptacle**

**Table 5: Lane Assignment**

| Fiber # | Lane Assignment |
|---|---|
| 1 | RX0 |
| 2 | RX1 |
| 3 | RX2 |
| 4 | RX3 |
| 5,6,7,8 | Not used |
| 9 | TX3 |
| 10 | TX2 |
| 11 | TX1 |
| 12 | TX0 |

## 6. Recommended Power Supply Filter

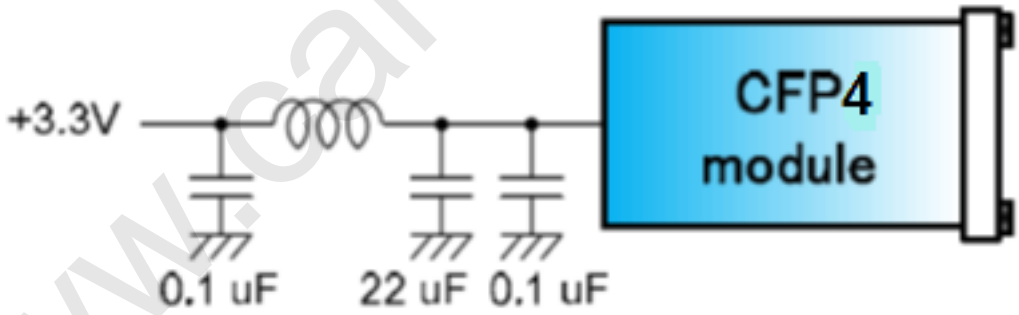



**Figure 4. Recommended Power Supply Filter**

## 7. Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | Ts | -40 | 85 | degC | |
| Relative Humidity (non-condensation) | RH | | 85 | % | |
| Operating Case Temperature | $T_{OP}$ | -5 | 70 | degC | |
| Supply Voltage | Vcc | -0.5 | 3.6 | V | |
| Voltage on LVTTL Input | Vilvttl | -0.5 | VCC3+0.3 | V | |
| LVTTL Output Current | Iolvttl | | 15 | mA | |
| Voltage on Open Collector Output | Voco | 0 | 6 | V | |
| Damage Threshold, each Lane | $TH_d$ | 3.4 | | dBm | 1 |

Notes:
1. PIN receiver.

## 8. Recommended Operating Conditions and Supply Requirements

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Operating Case Temperature | $T_{OP}$ | -5 | | 70 | degC | |
| Power Supply Voltage | $V_{CC}$ | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 25.78125 | | Gb/s | |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Control Input Voltage High | | 2 | | Vcc | V | |
| Control Input Voltage Low | | 0 | | 0.8 | V | |
| Power Supply Noise | Vrip | | | 2 | % | DC-1MHz |
| | | | | 3 | % | 1-10MHz |
| Link Distance (OM3 MMF) | D1 | | | 70 | m | |
| Link Distance (OM4 MMF) | D2 | | | 300 | m | |

## 9. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

| Parameter | Test Point | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Power Consumption | | | | 3.5 | W | |
| Supply Current | Icc | | | 1.06 | A | |
| Low Power Mode Power Dissipation | | | | 1.0 | W | |
| **Transmitter (each Lane)** | | | | | | |
| Overload Differential Voltage pk-pk | TP1a | 900 | | | mV | |
| Common Mode Voltage (Vcm) | TP1 | -350 | | 2850 | mV | 1 |
| Differential Termination Resistance Mismatch | TP1 | | | 10 | % | At 1MHz |
| Differential Return Loss (SDD11) | TP1 | | | See CEI-28G-VSR Equation 13-19 | dB | |
| Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11) | TP1 | | | See CEI-28G-VSR Equation 13-20 | dB | |
| Stressed Input Test | TP1a | See CEI-28G-VSR Section 13.3.11.2.1 | | | | |
| **Receiver (each Lane)** | | | | | | |
| Differential Voltage, pk-pk | TP4 | | | 900 | mV | |
| Common Mode Voltage (Vcm) | TP4 | -350 | | 2850 | mV | 1 |
| Common Mode Noise, RMS | TP4 | | | 17.5 | mV | |
| Differential Termination Resistance Mismatch | TP4 | | | 10 | % | At 1MHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| Differential Return Loss (SDD22) | TP4 | | | See CEI-28G-VSR | dB | |
| | | | | Equation 13-19 | | |
| Common Mode to Differential conversion and Differential to | TP4 | | | See CEI-28G-VSR Equation 13-21 | dB | |
| Common Mode Return Loss | TP4 | | | -2 | dB | 2 |
| Transition Time, 20 to 80% | TP4 | 9.5 | | | ps | |
| Vertical Eye Closure (VEC) | TP4 | | | 5.5 | dB | |
| Eye Width at 10-15 probability | TP4 | 0.57 | | | UI | |
| Eye Height at 10-15 probability | TP4 | 228 | | | mV | |

Notes:
1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. From 250MHz to 30GHz.

## 10. Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Center Wavelength | $\lambda_C$ | 840 | 850 | 860 | nm | |
| RMS Spectral Width | $\Delta\lambda_{rms}$ | | | 0.6 | nm | |
| Average Launch Power, each Lane | $P_{AVG}$ | -8.4 | | 2.4 | dBm | |
| Optical Modulation Amplitude (OMA), each Lane | $P_{OMA}$ | -6.4 | | 3.0 | dBm | 1 |
| Launch Power in OMA minus TDEC, each Lane | | -7.3 | | | dBm | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Transmitter and Dispersion Eye Closure (TDEC), each Lane | | | | 4.3 | dB | |
| Extinction Ratio | ER | 2.0 | | | dB | |
| Optical Return Loss Tolerance | TOL | | | 12 | dB | |
| Average Launch Power OFF | Poff | | | -30 | dBm | |
| Transmitter, each Lane | | | | | | |
| Encircled Flux | | ≥ 86% at 19 µm<br>≤ 30% at 4.5 µm | | | | |
| Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3} | | {0.3, 0.38, 0.45, 0.35, 0.41, 0.5} | | | | 2 |
| **Receiver** | | | | | | |
| Center Wavelength | $\lambda_C$ | 840 | 850 | 860 | nm | |
| Damage Threshold, each Lane | $TH_d$ | 3.4 | | | dBm | 3 |
| Average Receive Power, each Lane | | -10.3 | | 2.4 | dBm | |
| Receive Power (OMA), each Lane | | | | 3.0 | dBm | |
| Receiver Sensitivity (OMA), each Lane | SEN | | | -9.2 | dBm | for BER = $5x10^{-5}$ |
| Stressed Receiver Sensitivity (OMA), each Lane | | | | -5.2 | dBm | 4 |
| Receiver Reflectance | $R_R$ | | | -12 | dB | |
| LOS Assert | LOSA | -30 | | | dBm | |
| LOS Deassert | LOSD | | | -12 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| **Conditions of Stress Receiver Sensitivity Test (Note 5)** | | | | | | |
| Stressed Eye Closure (SEC), Lane under Test | | | 4.3 | | dB | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Stressed Eye J2 Jitter, Lane under Test | | | 0.39 | | UI | |
| Stressed Eye J4 Jitter, Lane under Test | | | | 0.53 | UI | |
| OMA of each Aggressor Lane | | | 3 | | dBm | |
| Stressed Receiver Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}, Hit ratio $5x10^{-5}$ hits per sample | | {0.28, 0.5, 0.5, 0.33, 0.33, 0.4} | | | | |

Notes:

1. Even if the TDP < 0.9 dB, the OMA min must exceed the minimum value specified here.
2. Hit ratio $1.5x10^{-3}$ hits per sample.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = $5x10^{-5}$.
5. Vertical eye closure penalty, stressed eye J2 jitter, stressed eye J4 jitter, and stressed receiver eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

**11. Digital Diagnostic Functions**

The following digital diagnostic characteristics are defined over the Recommended Operating Environment unless otherwise specified. It is compliant to SFF-8436.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Temperature monitor absolute error | DMI_Temp | -3 | 3 | degC | Over operating temperature range |
| Supply voltage monitor absolute error | DMI _VCC | -0.15 | 0.15 | V | Over full operating range |
| Channel RX power monitor absolute error | DMI_RX_Ch | -2 | 2 | dB | 1 |
| Channel Bias current monitor | DMI_Ibias_Ch | -10% | 10% | mA | Ch1~Ch4 |
| Channel TX power monitor absolute error | DMI_TX_Ch | -2 | 2 | dB | 1 |

Notes:
1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

## 12. Mechanical Dimensions

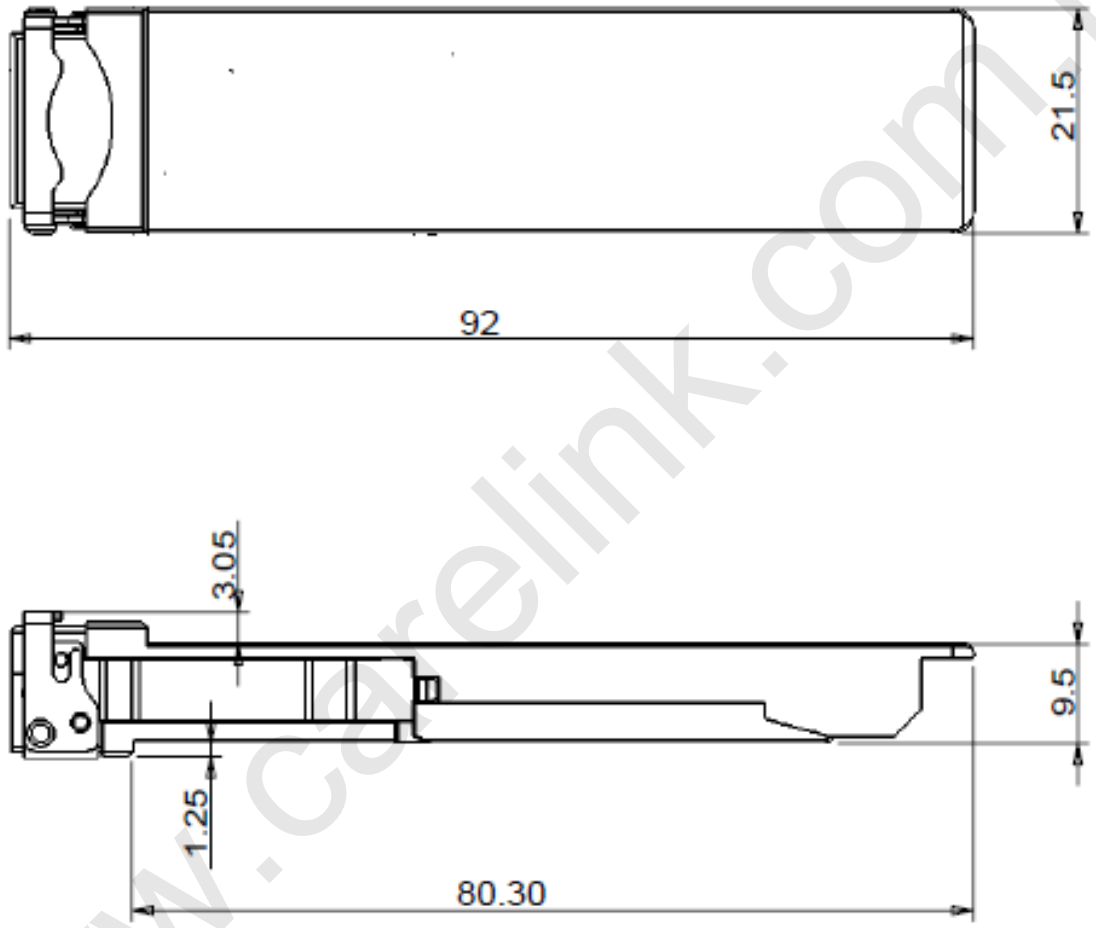



**Figure 5. Mechanical Outline**

**13. ESD**

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

**14. Laser Safety**

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.