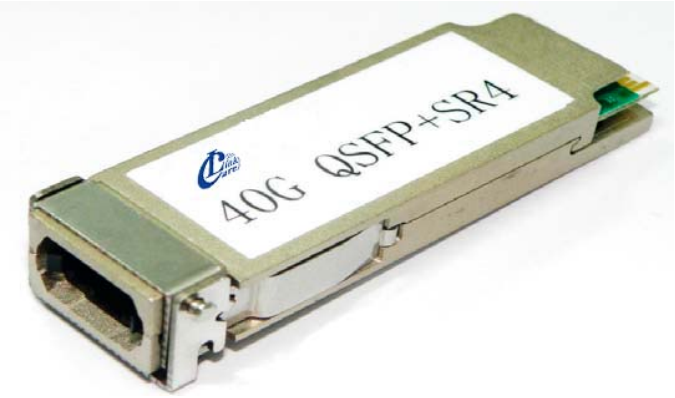
RoHS compliant
40Gb/s QSFP+ SR4 Optical Transceiver
40GBASE-SR4, up to 100m MM Fiber Link



Features

- 4 independent full-duplex channels
- Up to 11.2Gbps per channel bandwidth
- Aggregate bandwidth of > 40Gbps
- MTP/MPO optical connector
- QSFP MSA compliant
- Digital diagnostic capabilities
- Capable of over 100m transmission on high bandwidth 50um multi-mode ribbon fiber
- CML compatible electrical I/O
- Single +3.3V power supply, operating case temperature: 0~70C
- RoHS compliant
- TX input and RX output CDR retiming

Applications

- Rack to rack
- Data centers
- Metro networks
- Switches and Routers
- Infiniband 4x SDR, DDR, QDR
- 10G Ethernet

Ordering Information

PART NUMBER	INPUT/OUTPUT	SIGNAL DETECT	VOLTAGE	TEMPERATURE
CL-QSFP+_SR4	AC/AC	TTL	3.3V	0°C to 70 °C

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1.General Description

The CL-QSFP+_SR4 is a parallel 40Gbps Quad Small Form-factor Pluggable (QSFP) optical module that provides increased port density and total system cost savings. The QSFP full-duplex optical module offers 4 independent transmit and receive channels, each capable of 10Gbps operation for an aggregate bandwidth of 40Gbps over 100 meters of multi-mode fiber.
An optical fiber ribbon cable with an MPO/MTP™ connector at each end plugs into the QSFP module receptacle. The orientation of the ribbon cable is "keyed" and guide pins are present inside the module's receptacle to ensure proper alignment. The cable usually has no twist (key up to key up) to ensure proper channel to channel alignment. Electrical connection is achieved though a z-pluggable 38-pin IPASS® connector.
The module operates from a single +3.3V power supply and LVCMOS/LVTTL global control signals such as Module Present, Reset, Interrupt and Low Power Mode are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals and to obtain digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.
The CL-QSFP+_SR4 is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

2. Functional Description

The CL-QSFP+_SR4 converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) array into parallel optical output signals. The transmitter module accepts electrical input signals which are voltage compatible with Common Mode Logic (CML) levels. All input data signals are differential and are internally terminated. The receiver module converts parallel optical input signals via a receiver and a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals, which are voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 10 Gbps per channel. Figure 1 shows the functional block diagram of the CL-QSFP+_SR4 QSFP Transceiver.
A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.
Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP module must be used.
Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP memory map.
The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.
Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a "Low" state.
Interrupt (IntL) is an output pin. "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. Transceiver Block Diagram

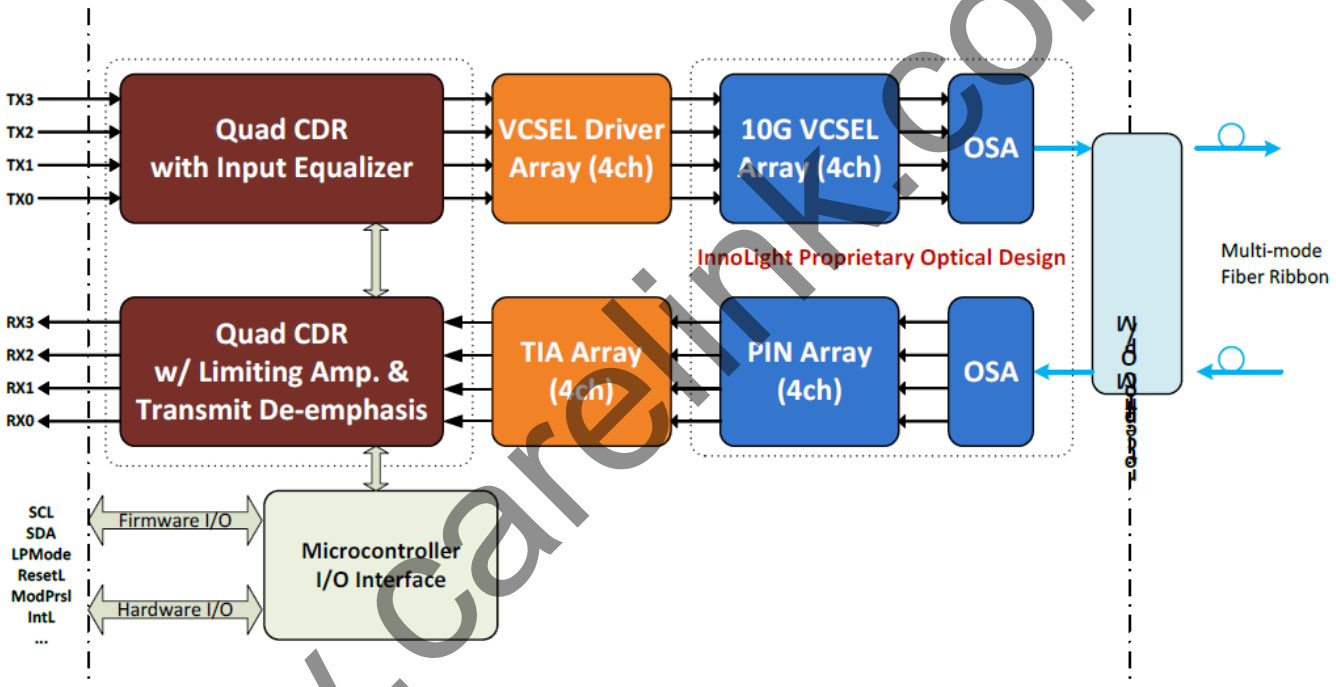


Figure 1 : QSFP Transceiver Block Diagram

Pin Assignment and Pin Description

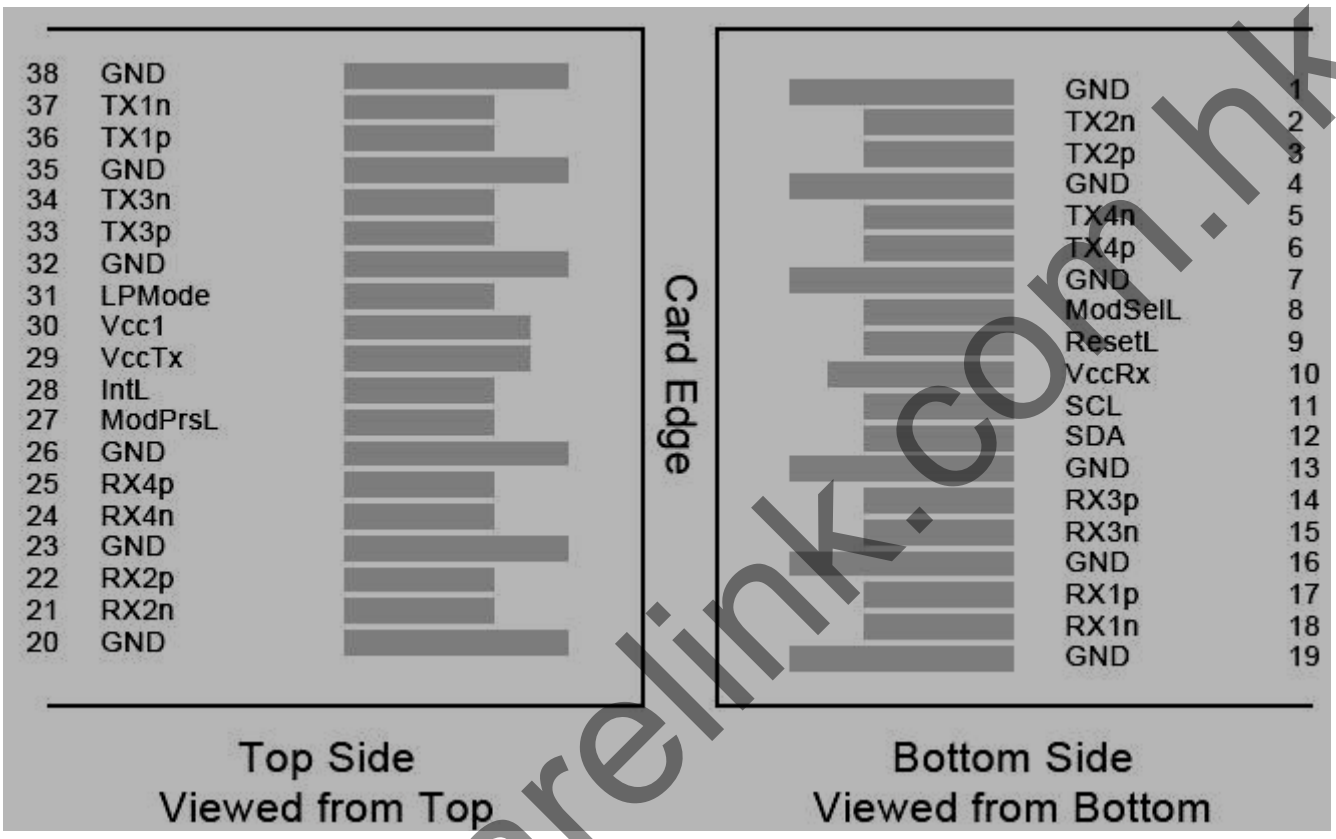


Figure 2: QSFP Transceiver Electrical Pad Layout

Pin Definitions.

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Optical Interface Lanes and Assignment

Figure 3 shows the orientation of the multi-mode fiber facets of the optical connector. Table 1 provides the lane assignment.

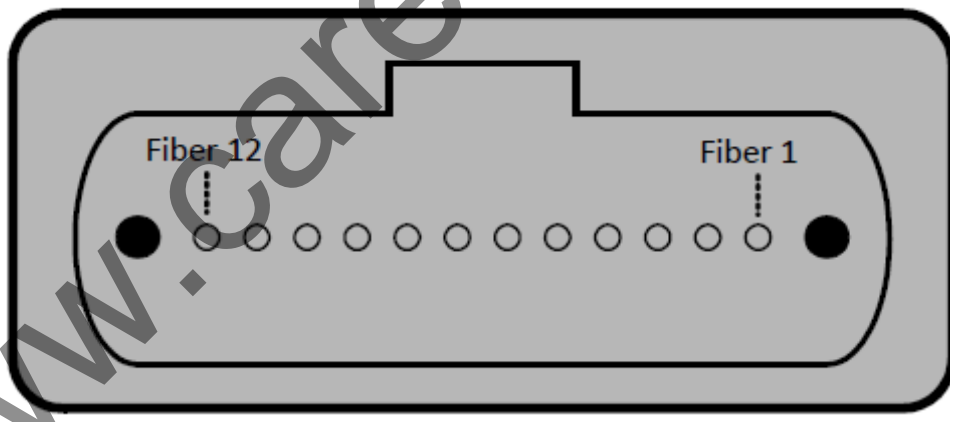


Figure 3: Outside view of the QSFP module MPO

Table1: lane assignment

Fiber #	Lane Assignment
1	RX0
2	RX1
3	RX2
4	RX3
5	Not used
6	Not used
7	Not used
8	Not used
9	TX3
10	TX2
11	TX1
12	TX0

Recommended Power Supply Filter

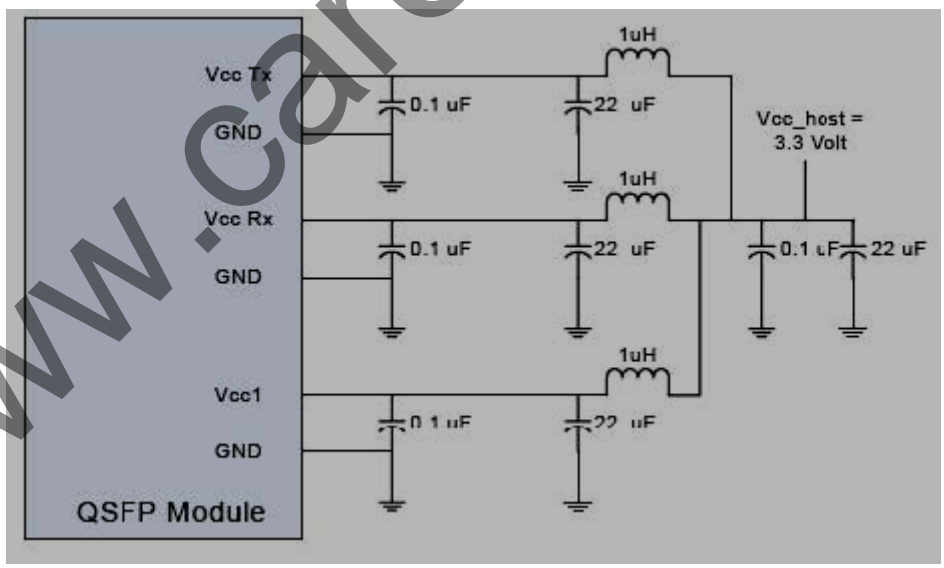


Figure 4 Recommended Power Supply Filter

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-20	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Operating Case Temperature	Topc	0	70	degC	1
Supply Voltage	VCC	-0.5	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC+0.5	V	
LVTTL Output Current	Iolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power(Average)	Mip		2	dBm	2

Notes:
1. Ta: -10 to 60degC with 1.5m/s airflow with an additional heat sink.
2. Pin Receiver.

5. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Topc	0	70	degC
Relative Humidity (non-condensing)	Rhop	-	85	%
Power Supply Voltage	VCC	3.1	3.5	V
Power Supply Current	ICC	-	1000	mA
Total Power Consumption	Pd	-	3.5	W

6. Optical Characteristics

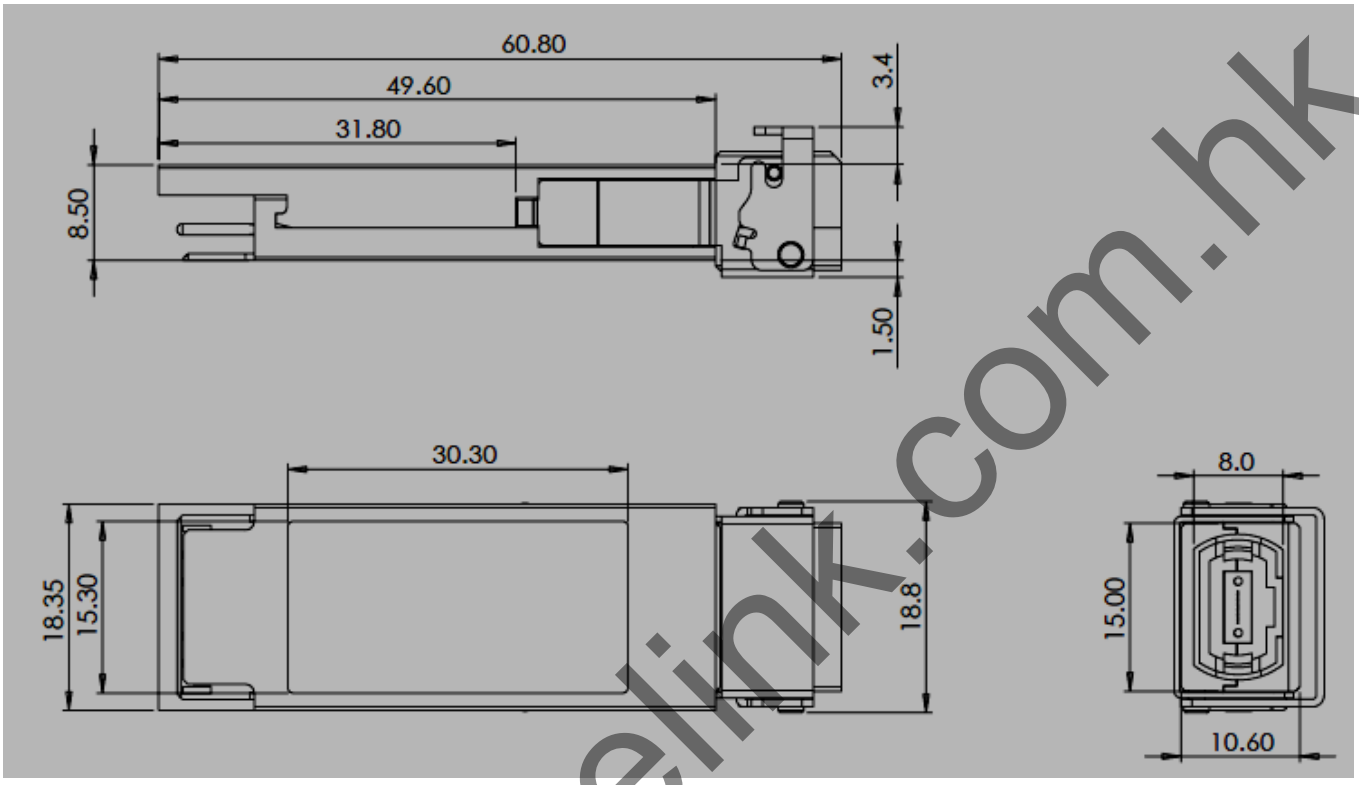
Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Transmitter						
Center Wavelength	λt	840	850	860	nm	
RMS Spectral Width	Pm	-	0.5	0.65	nm	
Average Optical Power per Channel	Pavg	-8	-2.5	+1	dBm	
Optical Power OMA	Poma	-6	-	+3	dBm	
Laser Off Power per Channel	Poff	-	-	-30	dBm	
Extinction Ratio	ER	3	-	-	dB	
Relative Intensity Noise	Rin	-	-	-128	dB/Hz	12dB reflection
Optical Return Loss Tolerance		-	-	12	dB	
Receiver						
Center Wavelength	λr	830	850	860	nm	
Receiver Sensitivity per Channel	Psens	-	-13		dBm	
Stressed Sensitivity per Channel		-	-	-5.4	dBm	
Los Assert	LosA	-30	-	-	dBm	
Los Dessert	LosD	-	-	-14	dBm	
Los Hysteresis	LosH	0.5	-	-	dB	
Overload	Pin	+1	-	-	dBm	
Receiver Reflectance		-	-	-12	dB	

7. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Data Rate per Channel		-	10.3125	11.2	Gbps	
Power Consumption		-	2.5	3.5	W	
Supply Current	ICC		0.75	1.0	A	
Control I/O Voltage, High	VIH	2.0		VCC	V	
Control I/O Voltage, Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			150	ps	
RESETL Duration			10		us	
RESETL De-assert time				100	ms	
Power on time				100	ms	
Transmitter						
Single Ended Output Voltage Tolerance		-0.3	-	4	V	
Common mode voltage tolerance		15	-	-	mV	
Tx Input Diff Voltage	VI	90		1600	mV	
Tx Input Diff Impedance	ZIN	80	100	120	Ω	
Data Dependent Input Jitter	DDJ			0.1	UI	
Data Input Total Jitter	TJ			0.28	UI	
Receiver						
Single Ended Output Voltage Tolerance		-0.3	-	4	V	
Rx Output Diff Voltage	Vo		600	800	mV	
Rx Output Rise and Fall Time	Tr/Tf			35	ps	20% to 80%
Total Jitter	TJ			0.7	UI	
Deterministic Jitter	DJ			0.42	UI	

8. Mechanical Dimensions



9. ESD

This transceiver is specified as ESD threshold 2kV for all electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

10. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (July 26, 2001)